

FIG. 1A

ASYNCHRONOUS SUBACTION

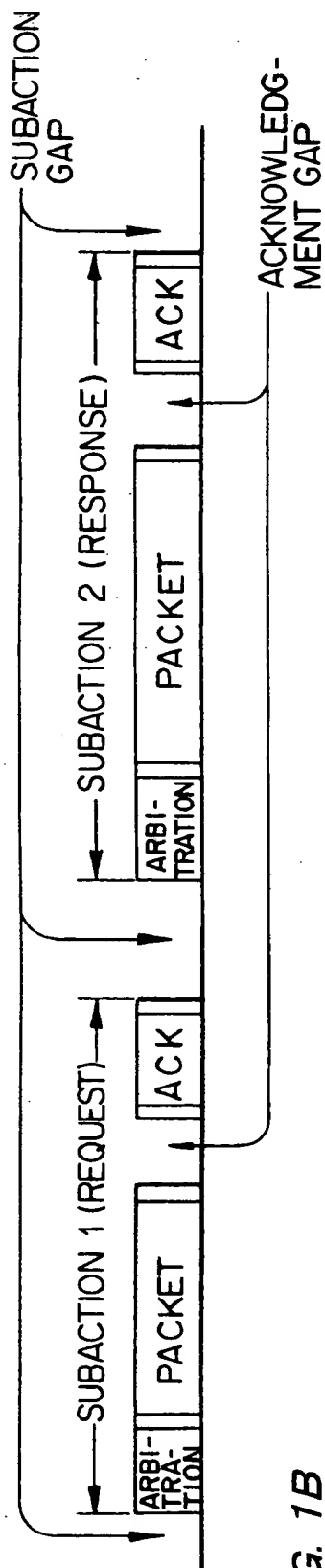


FIG. 1B

ISOSYNCHRONOUS SUBACTION

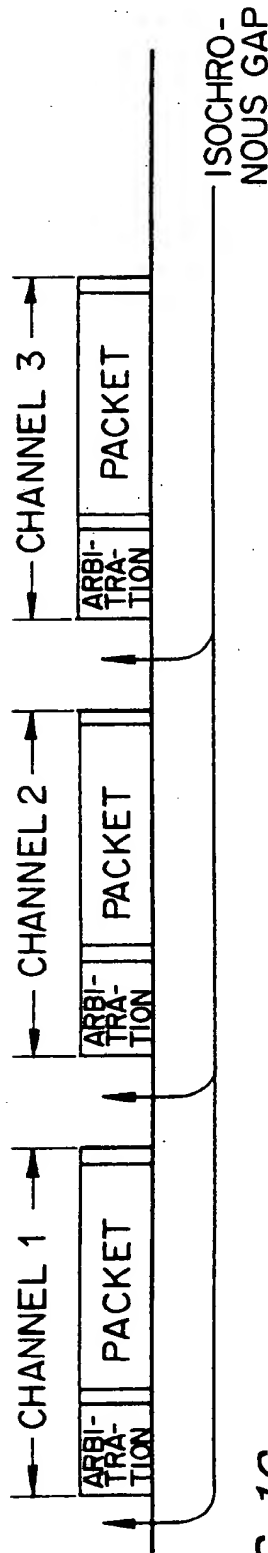


FIG. 1C

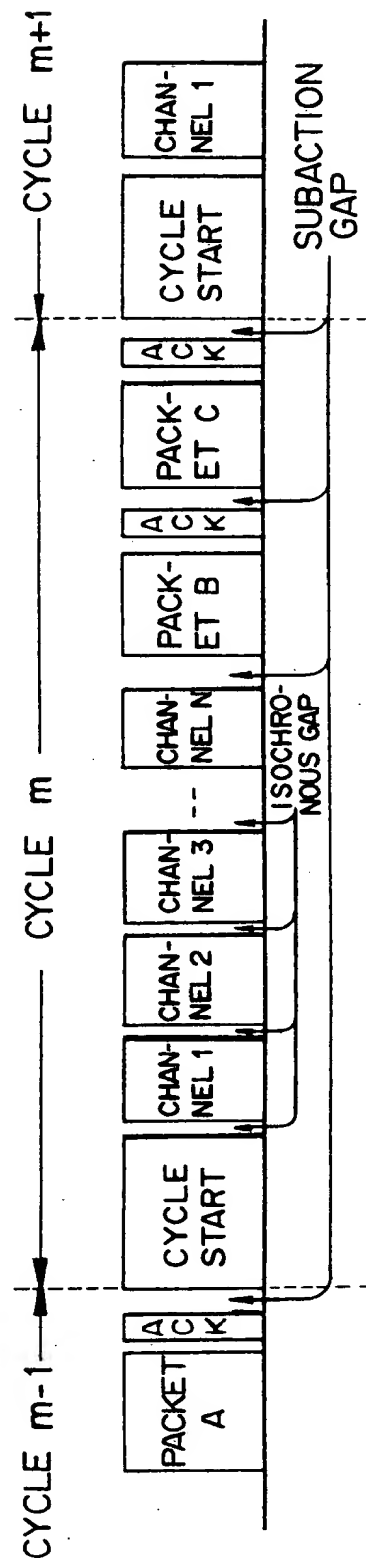


FIG. 2A

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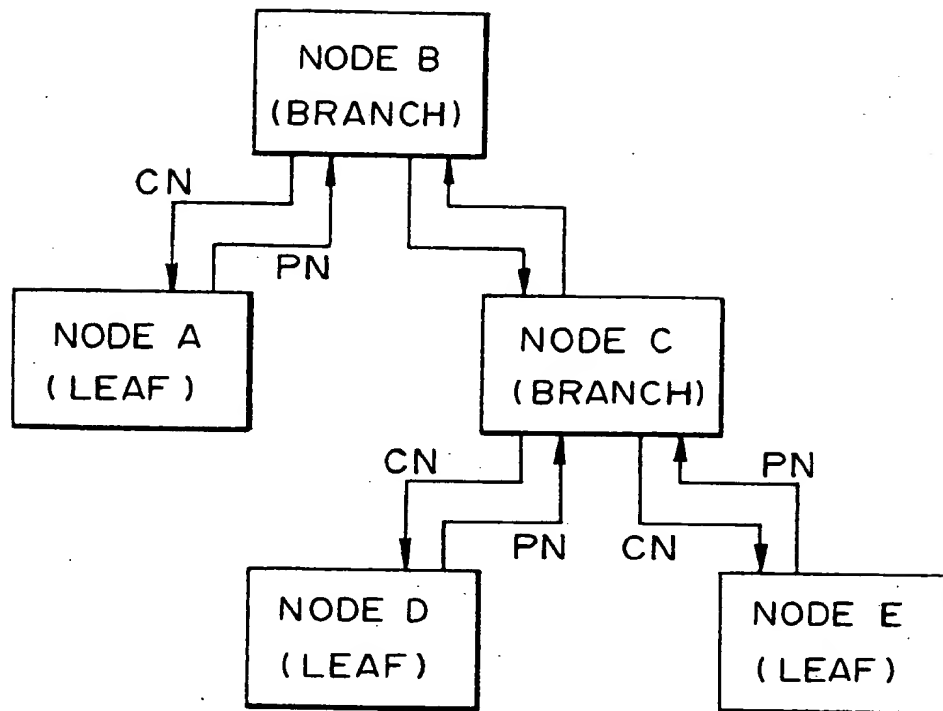


FIG. 2B

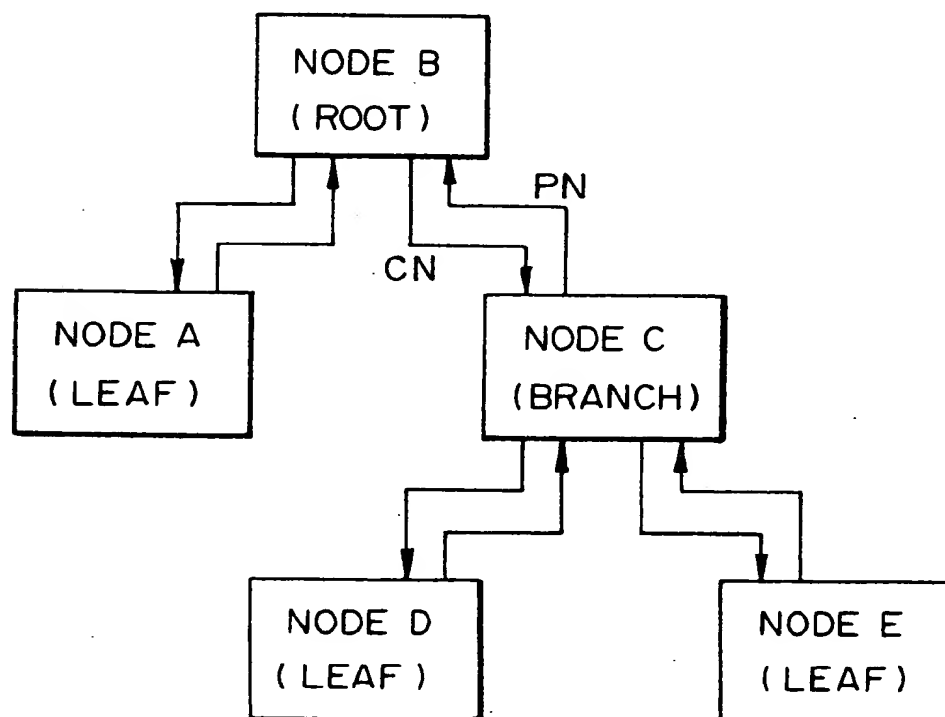
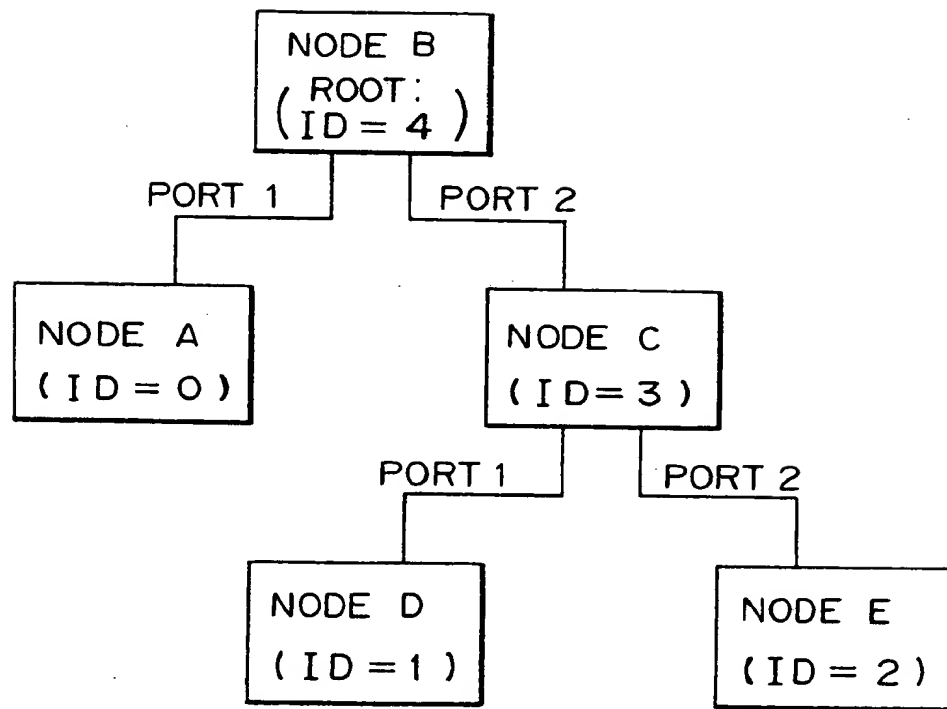
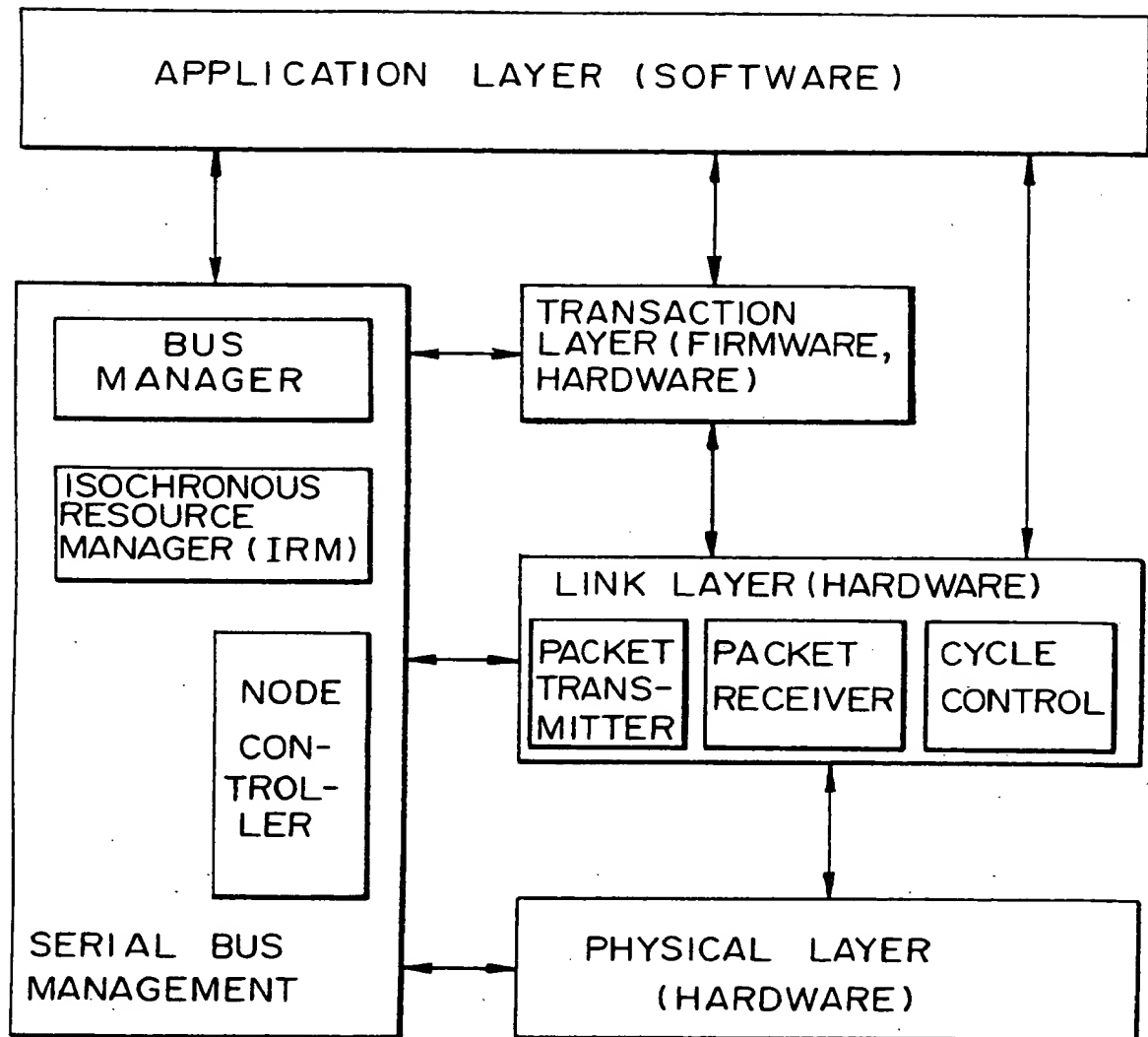


FIG. 3



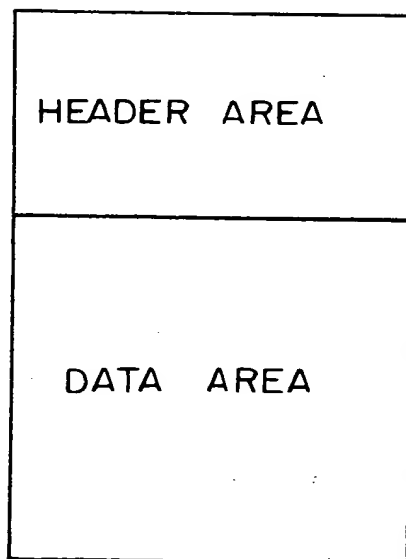
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FIG. 5



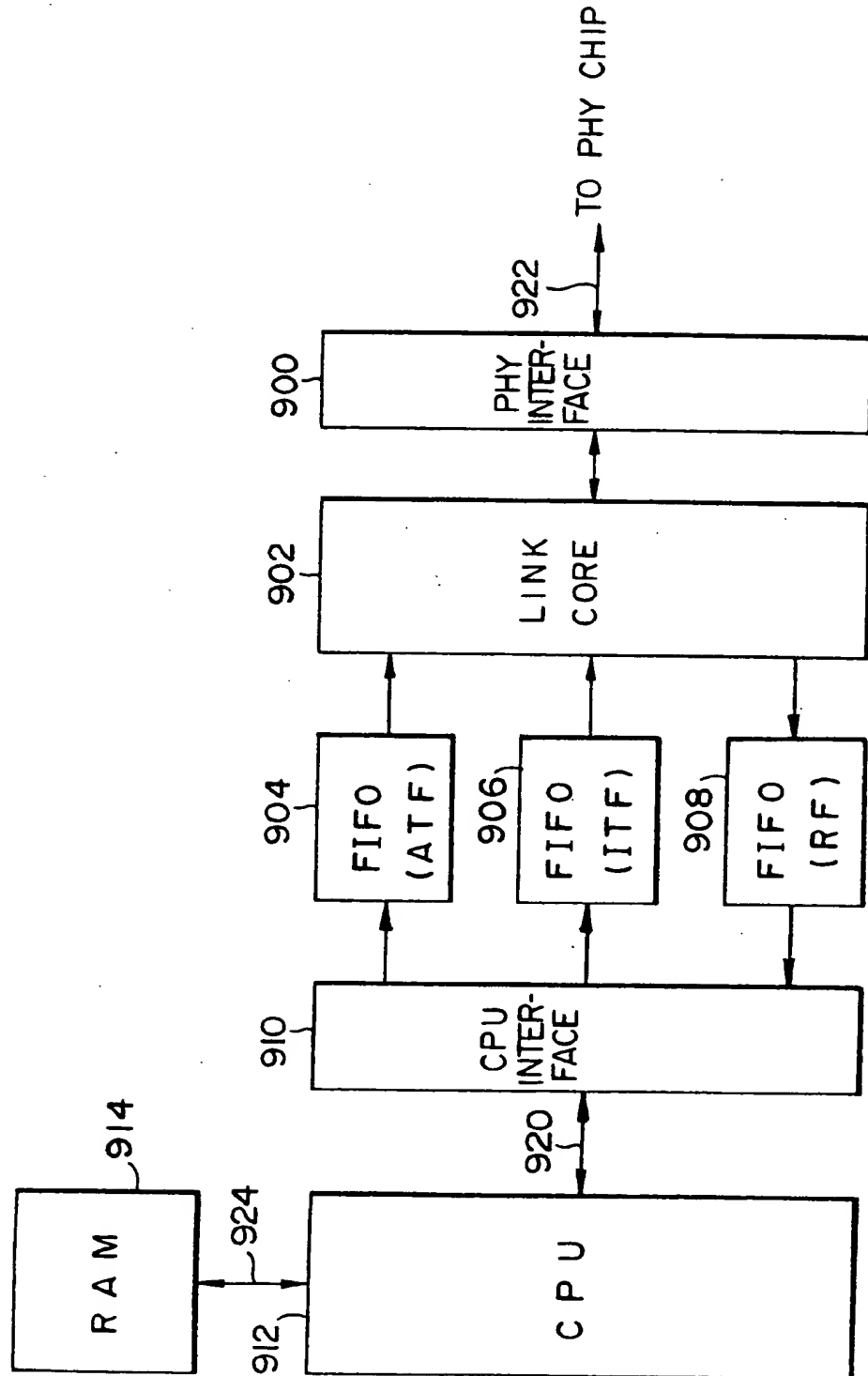
[illegible]

FIG. 7



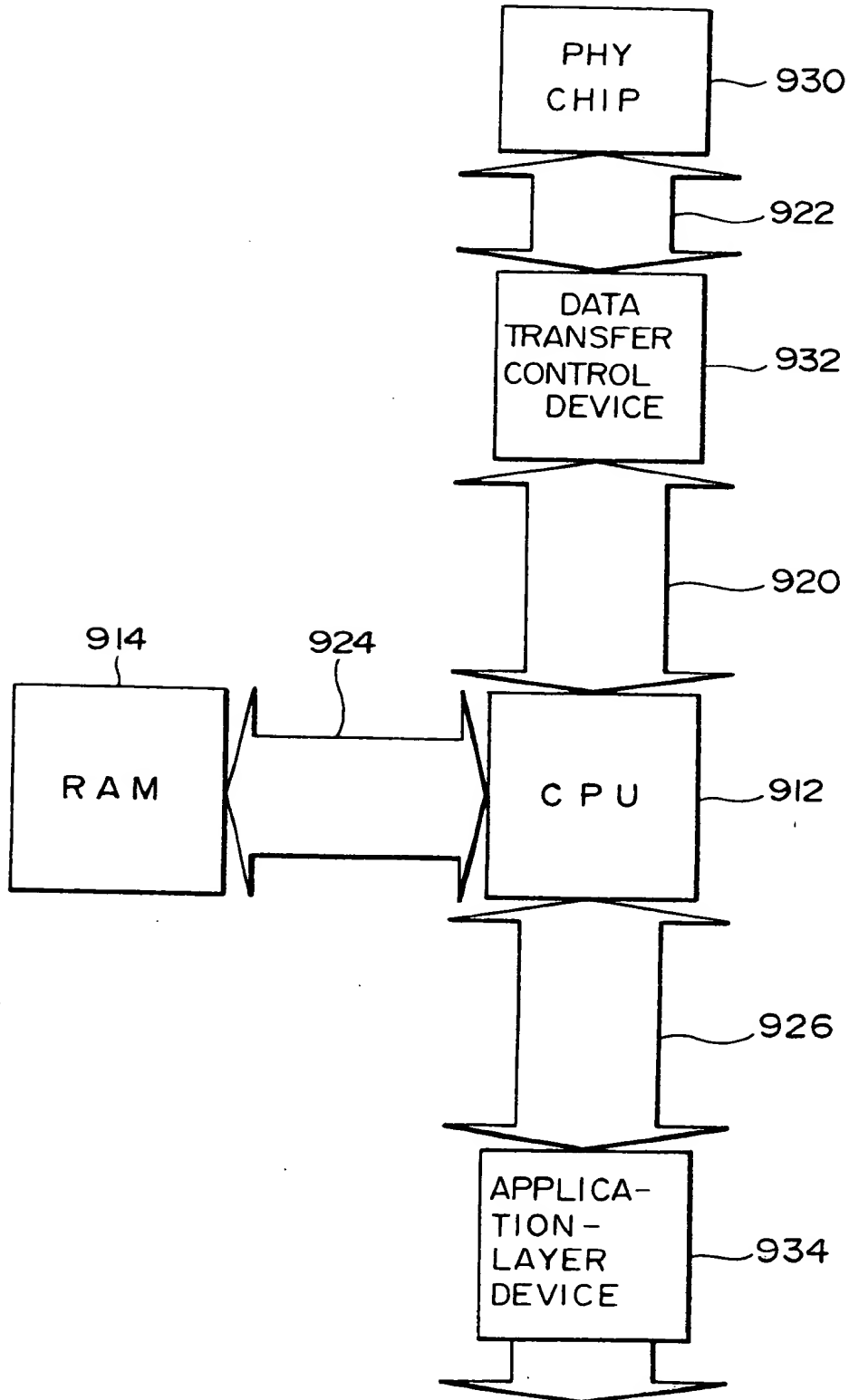
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FIG. 8



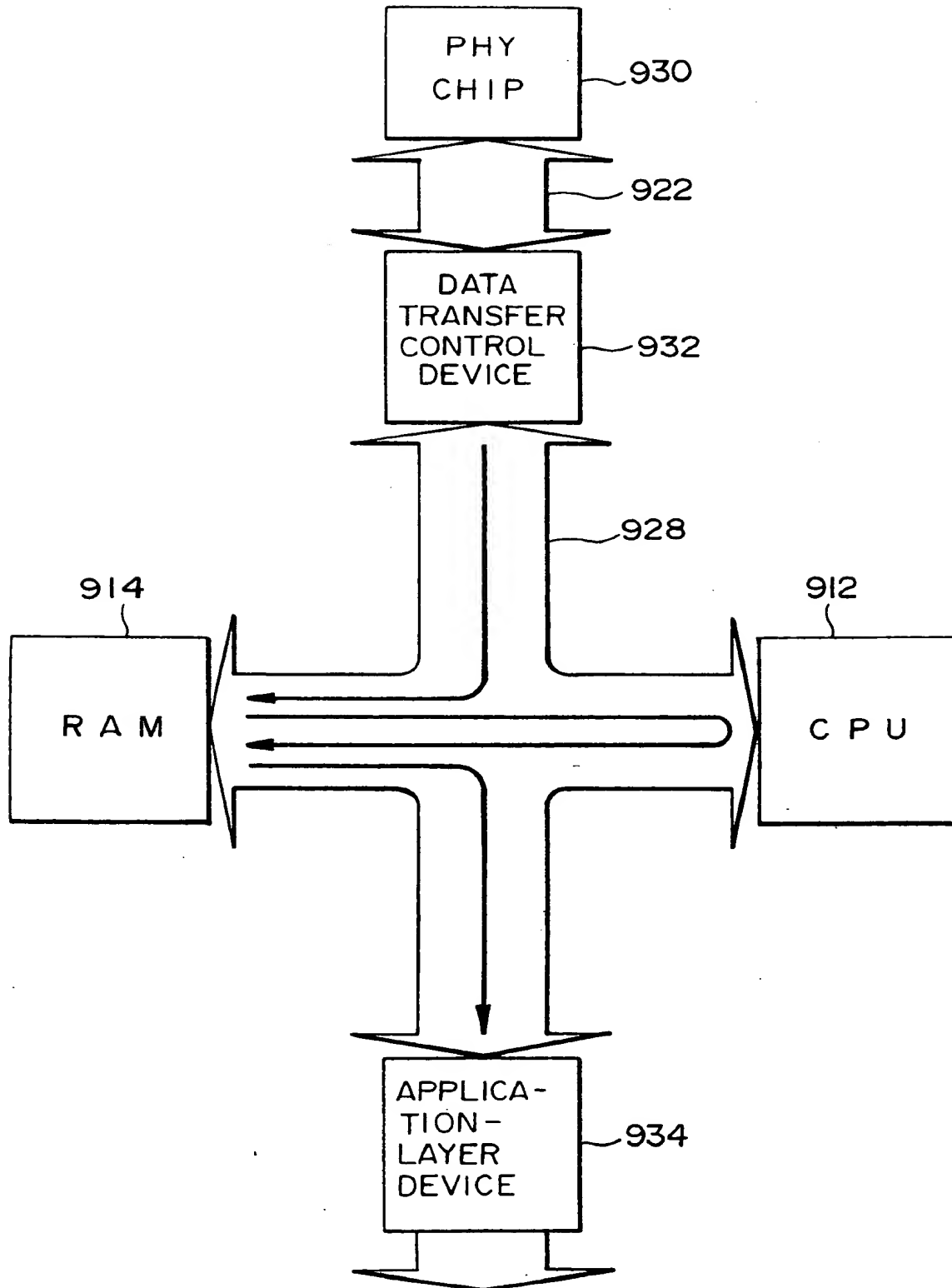
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FIG. 9



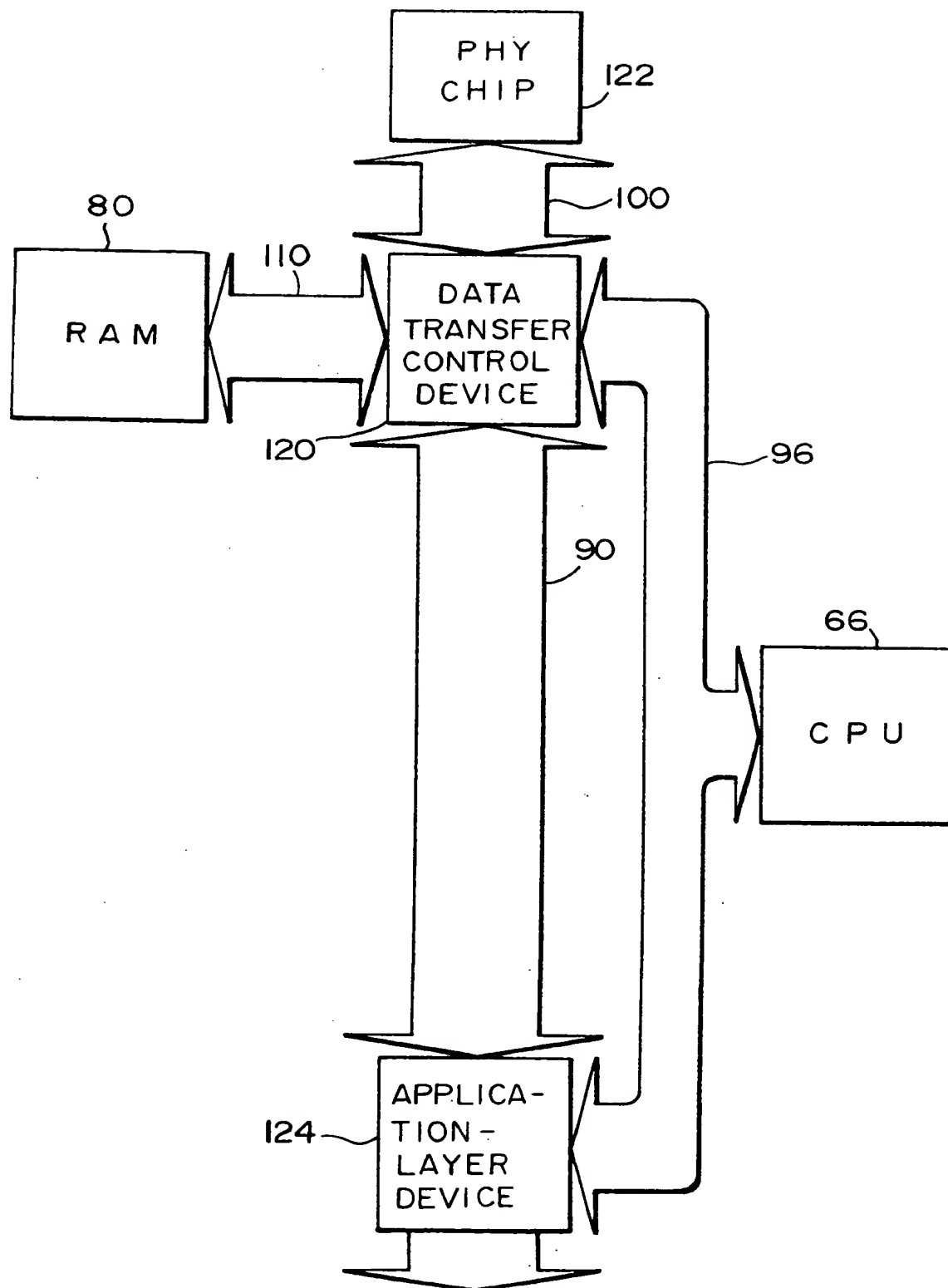
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FIG. 10



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FIG. 11



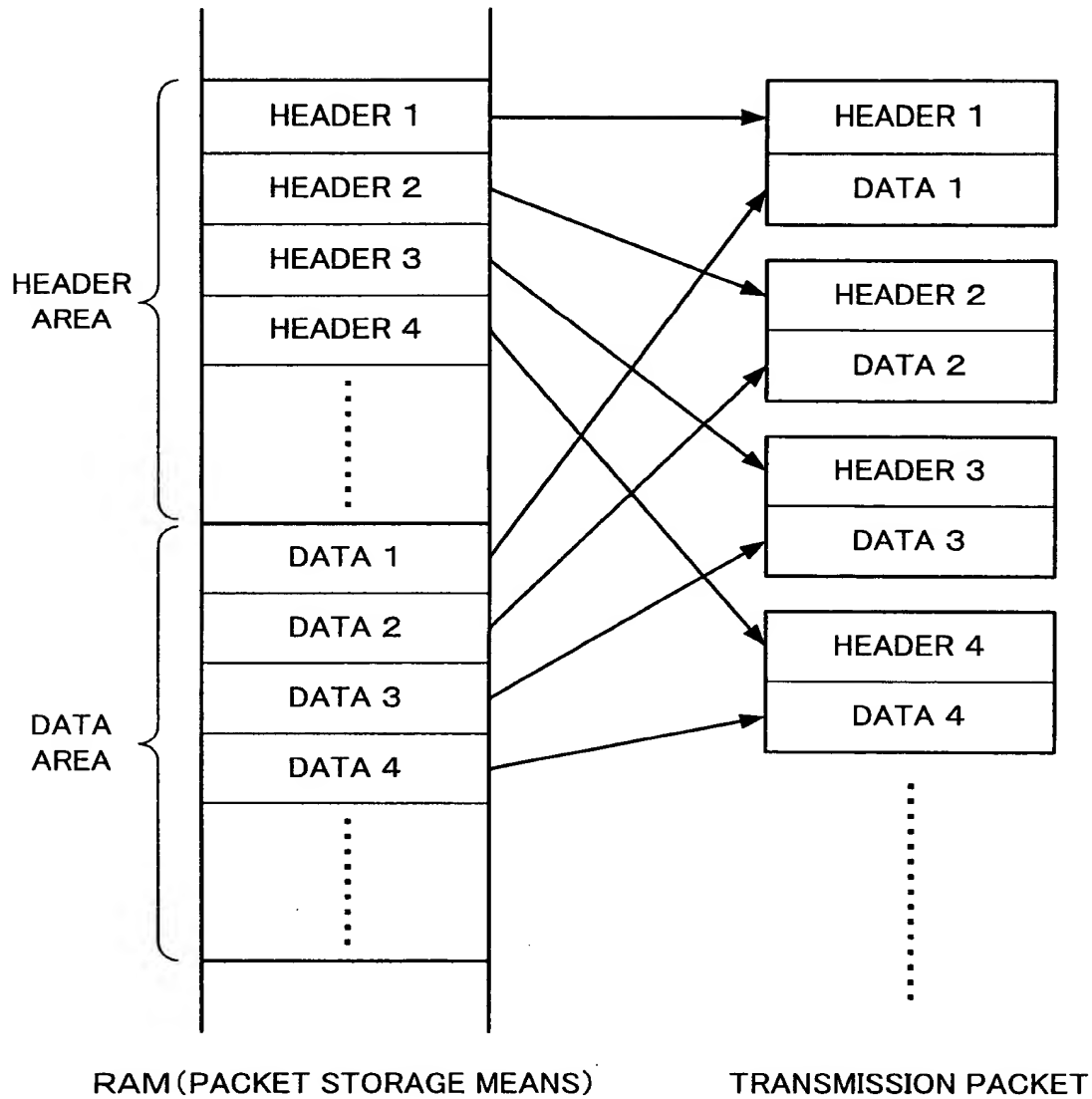


FIG. 13

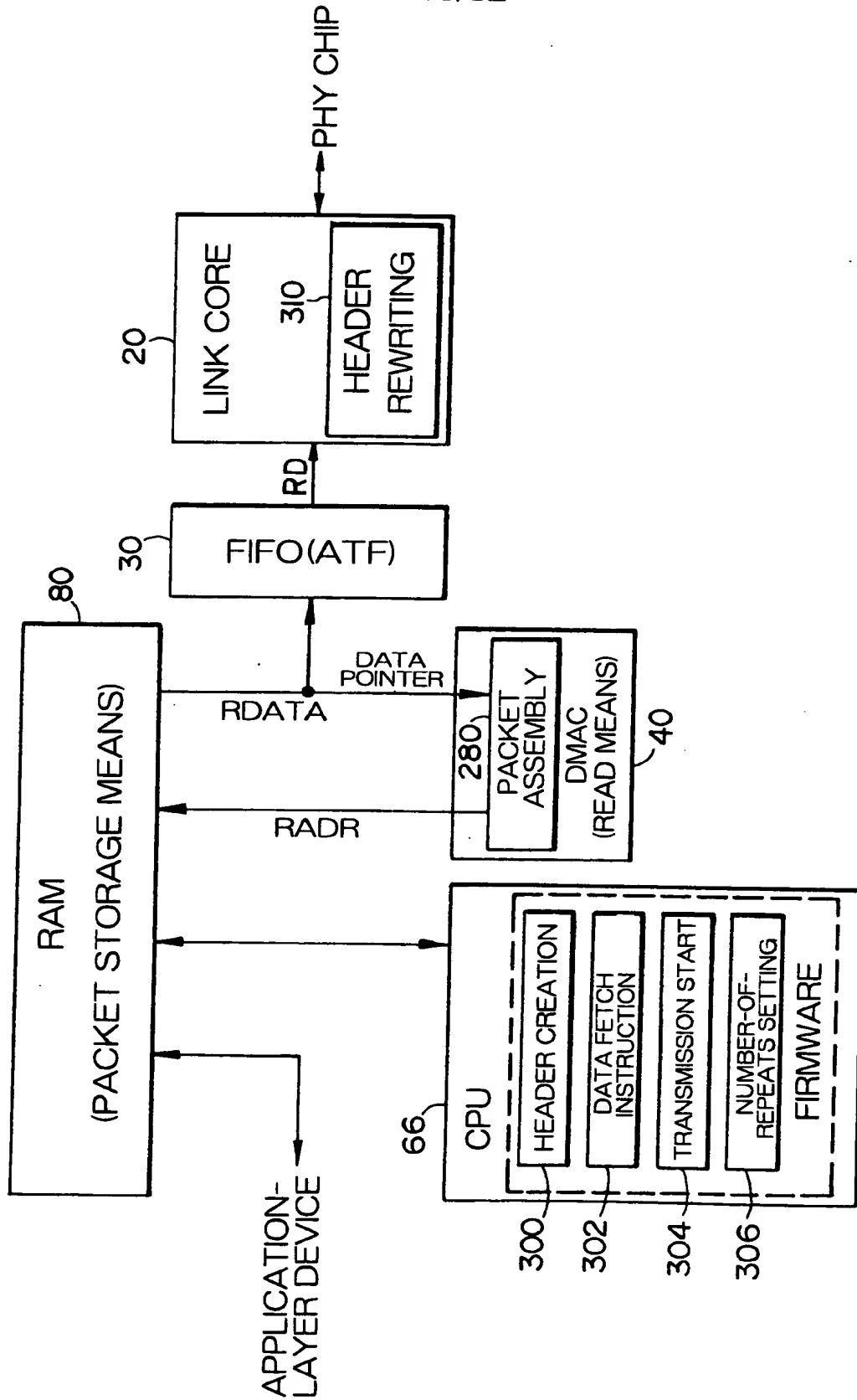
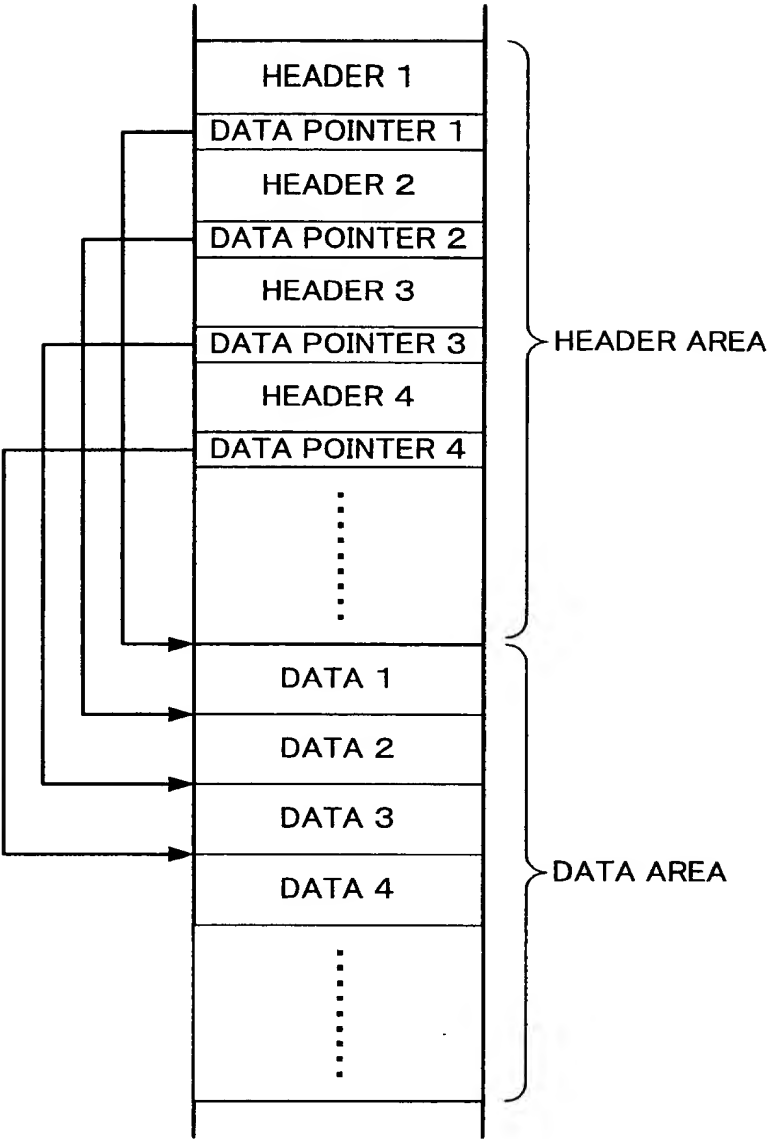


FIG. 14

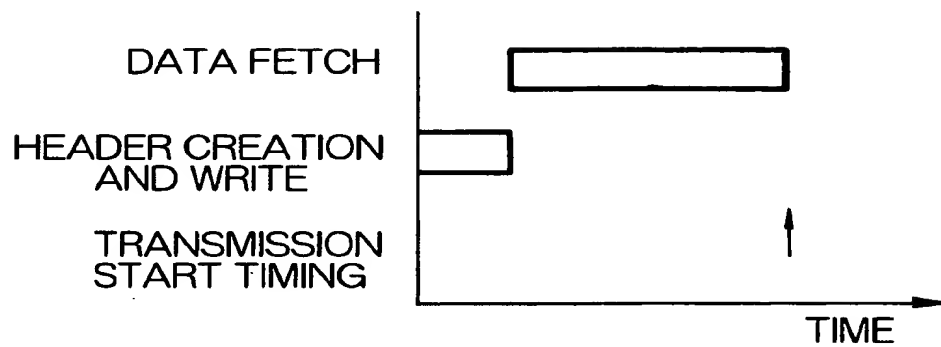


RAM(PACKET STORAGE MEANS)

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FIG. 15A

COMPARATIVE EXAMPLE

**FIG. 15B**

THIS EMBODIMENT

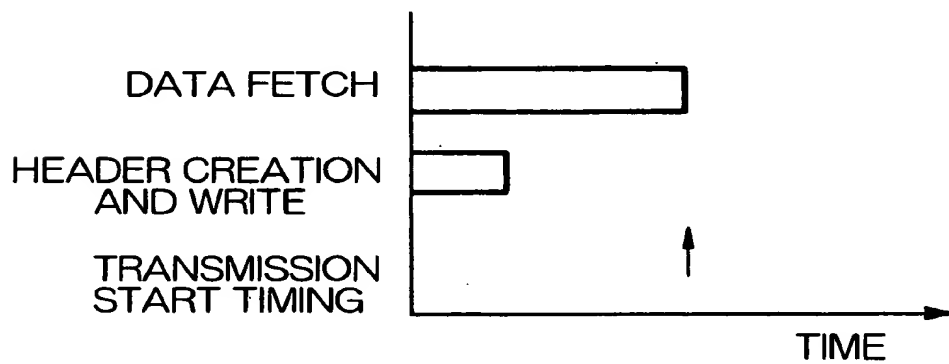


FIG. 16A

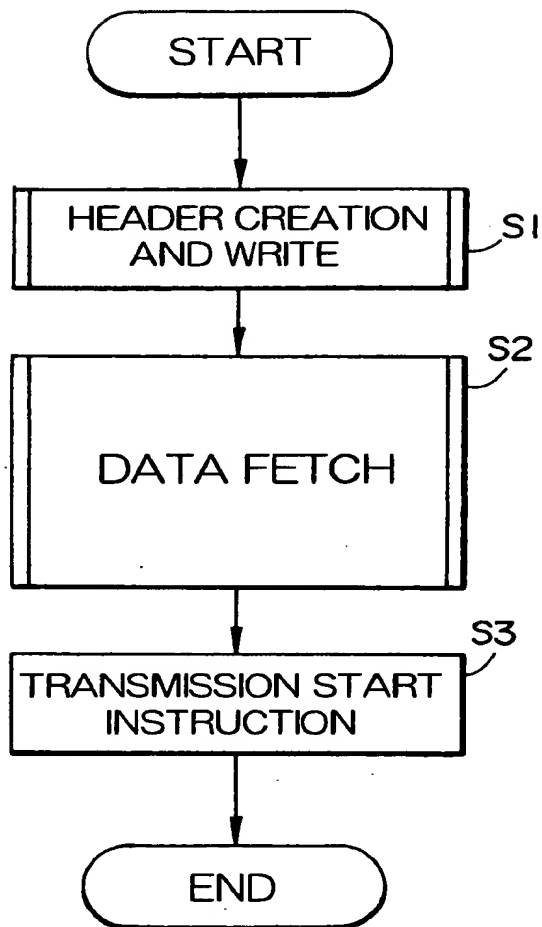


FIG. 16B

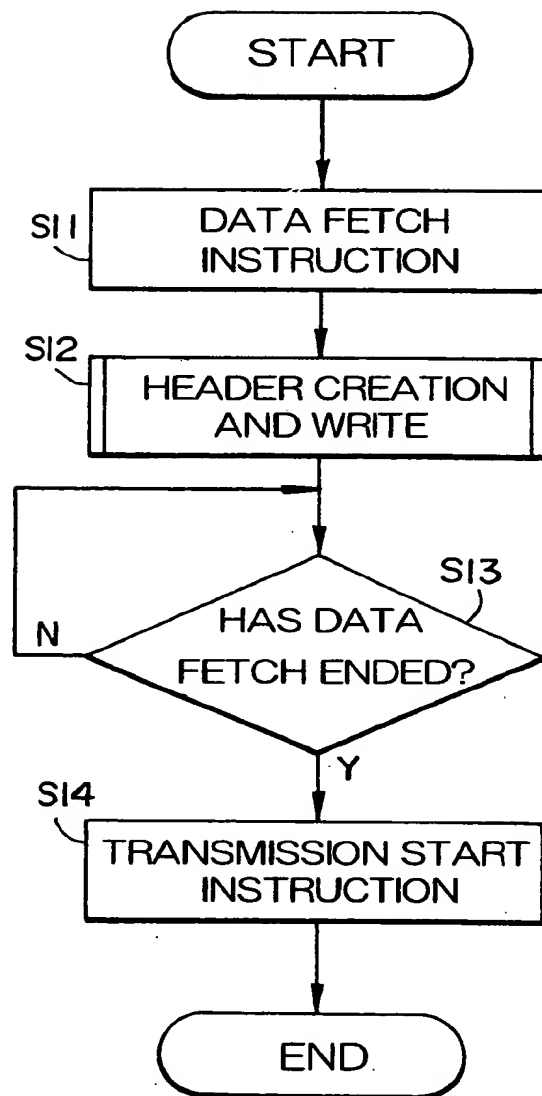


FIG. 17

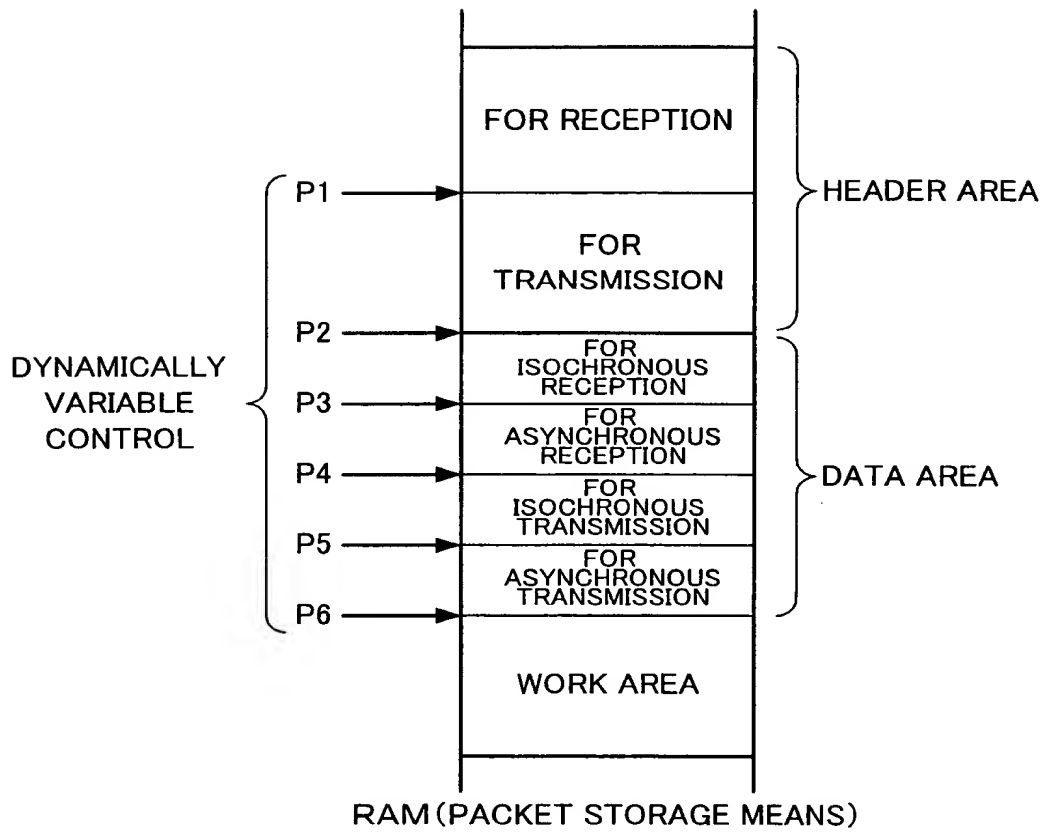


FIG. 18B

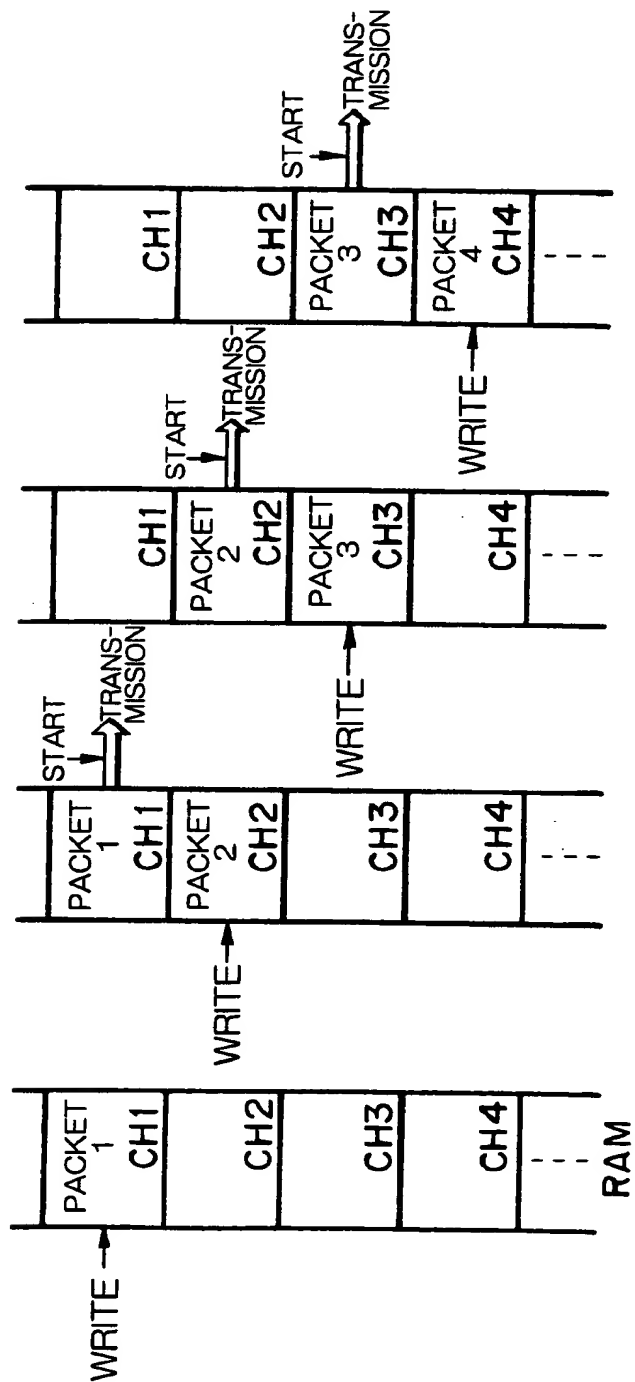
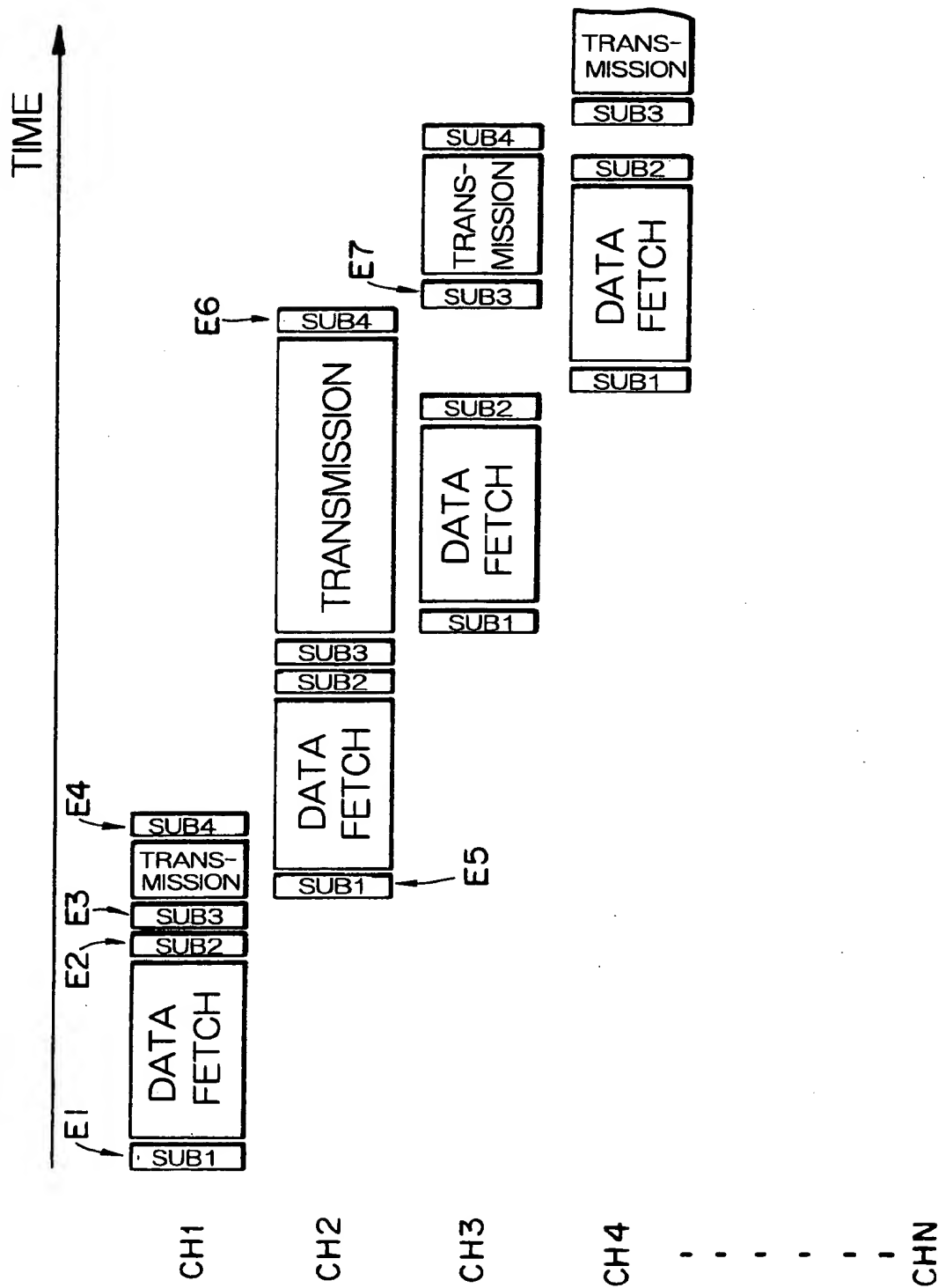


FIG. 19



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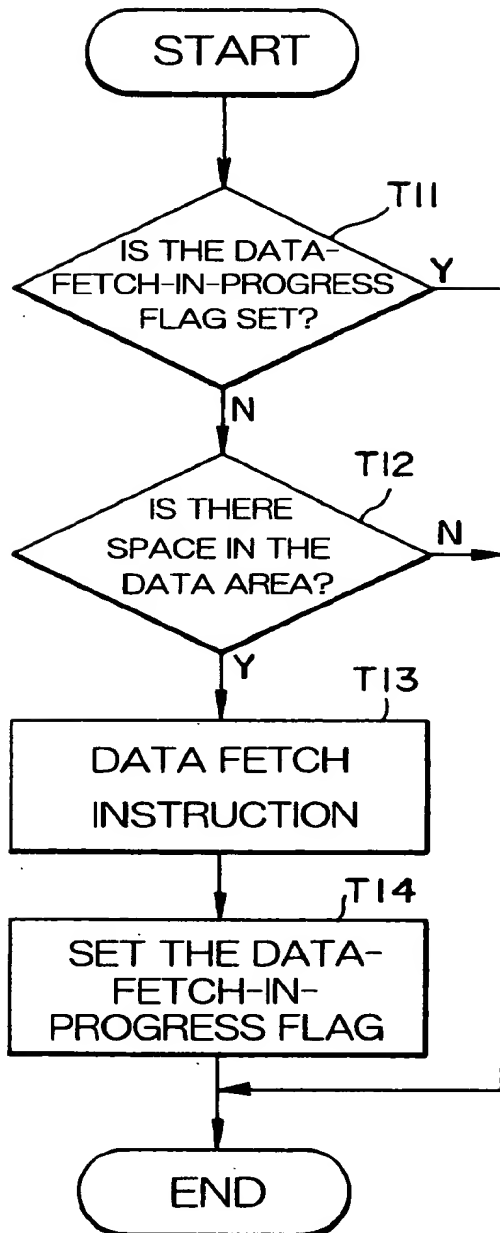
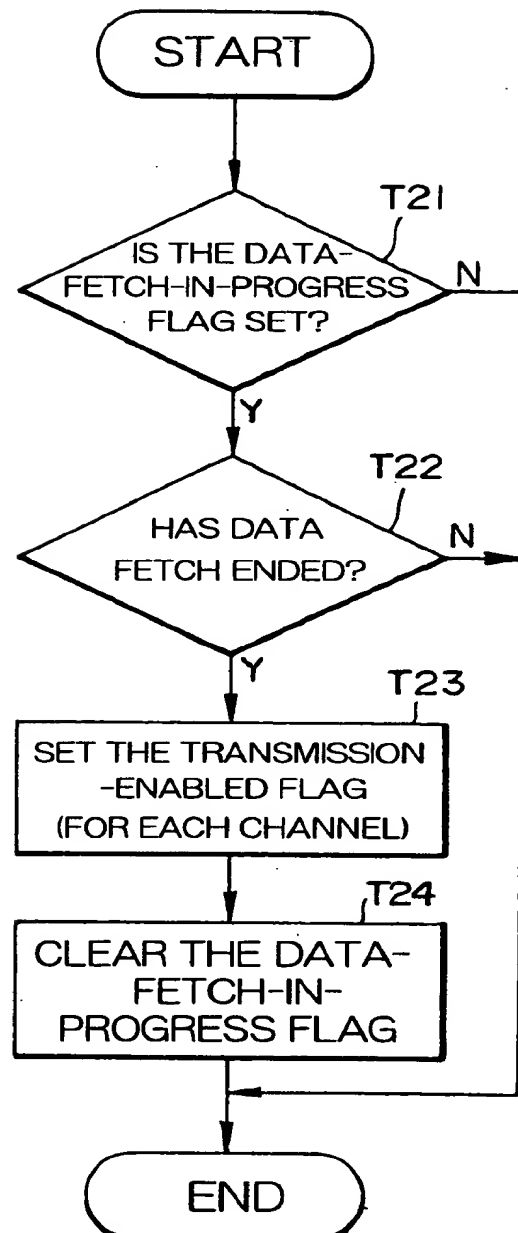
FIG. 20A
SUB 1FIG. 20B
SUB 2

FIG. 21B
SUB4

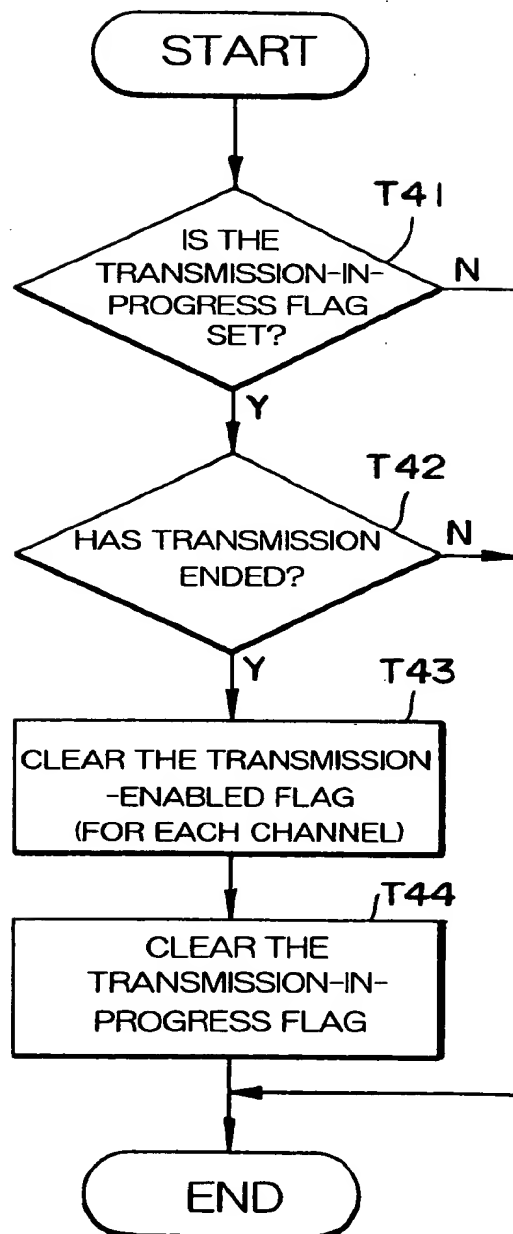


FIG. 22A

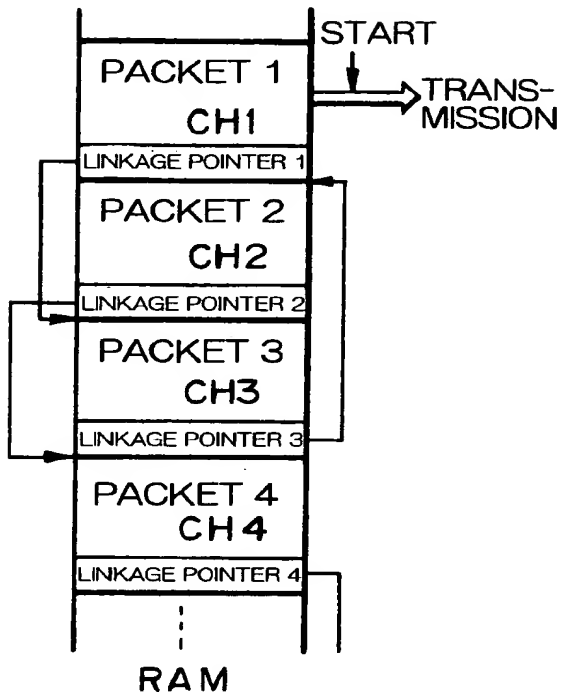


FIG. 22B

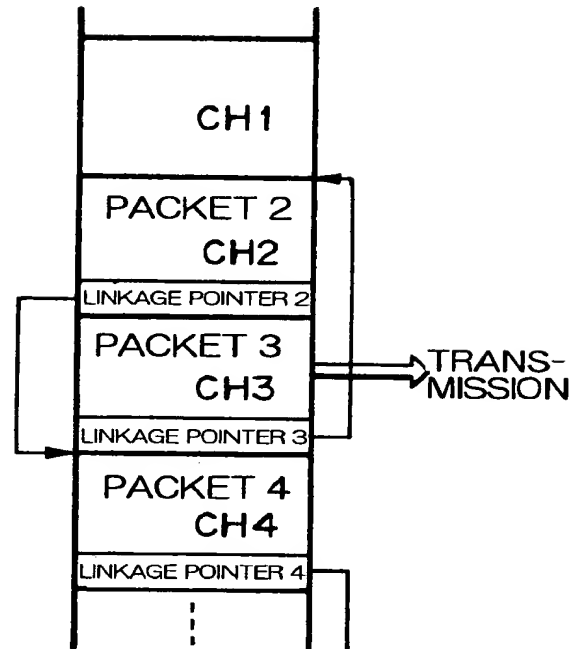


FIG. 22C

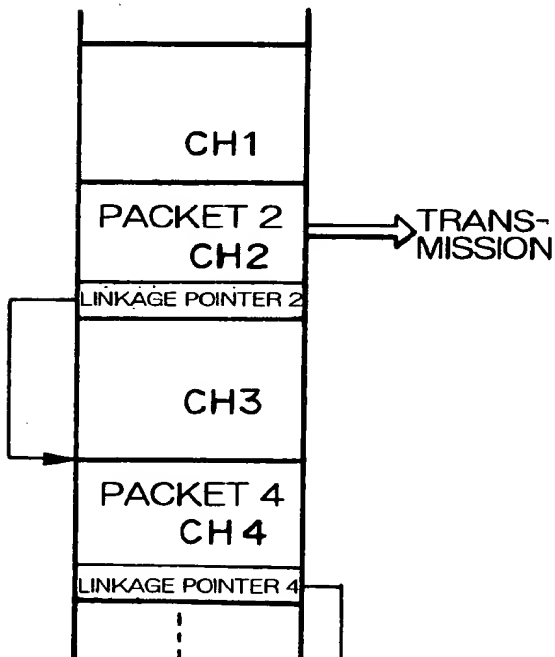


FIG. 22D

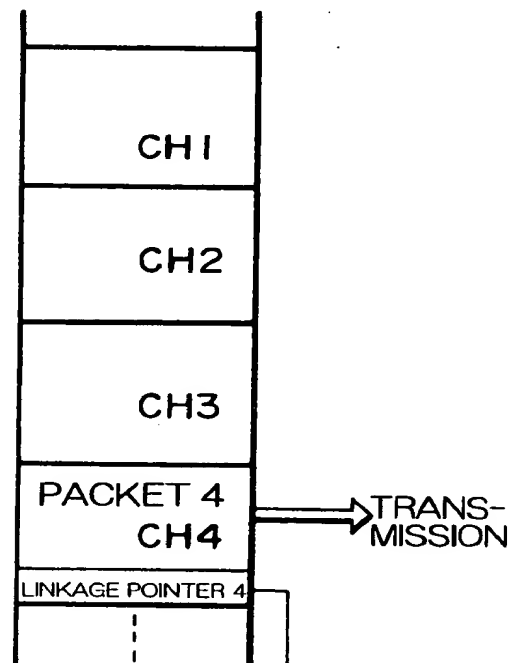


FIG. 23A

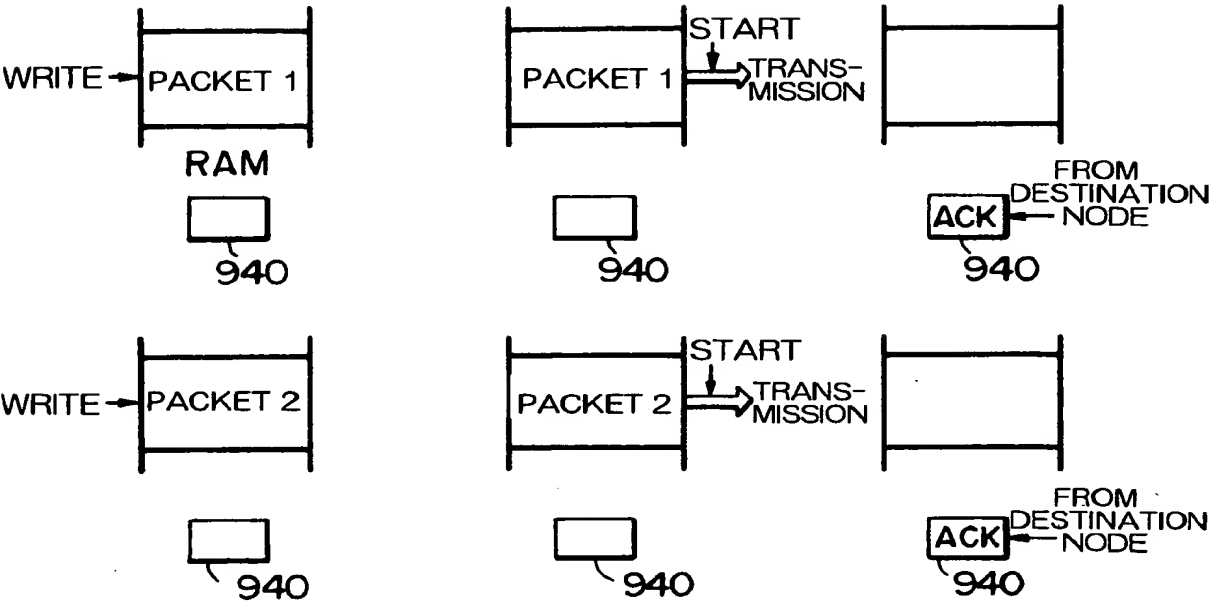


FIG. 23B

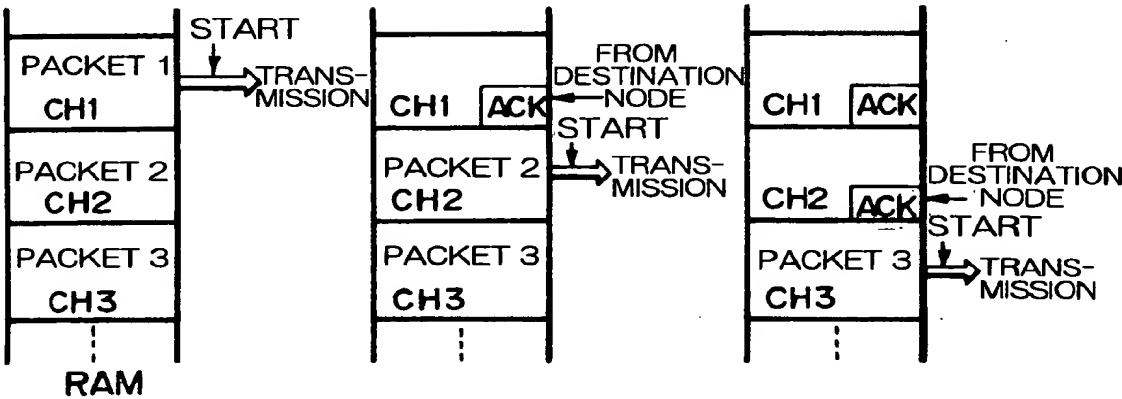


FIG. 23C

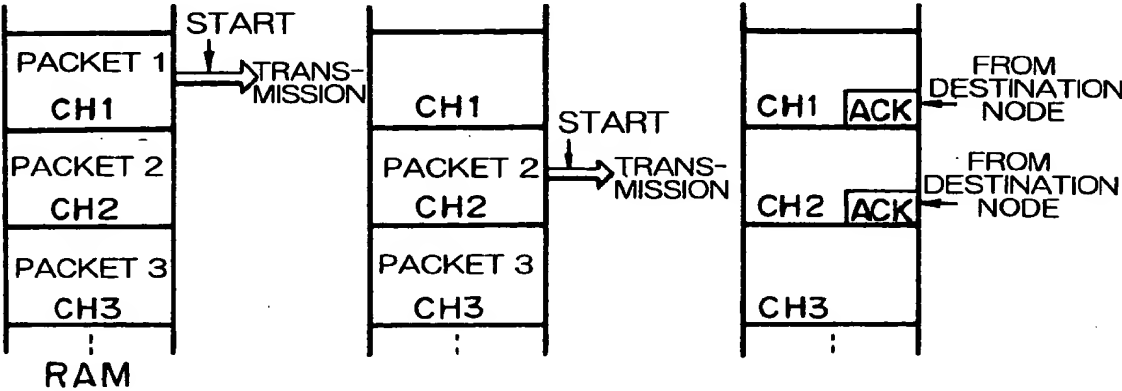


FIG. 24A

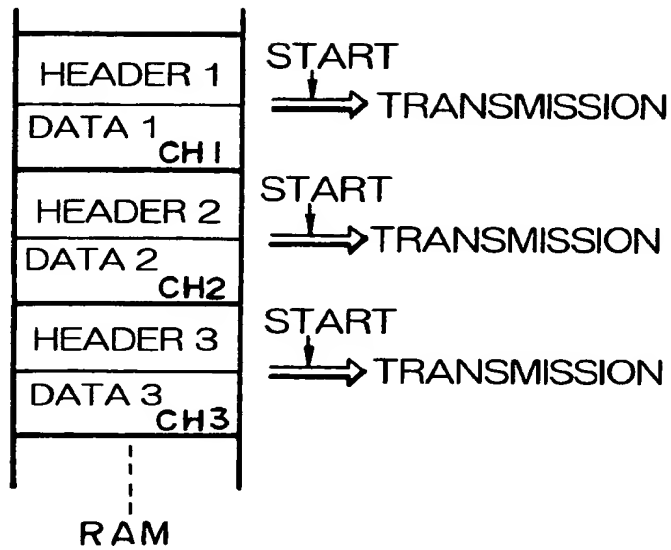


FIG. 24B

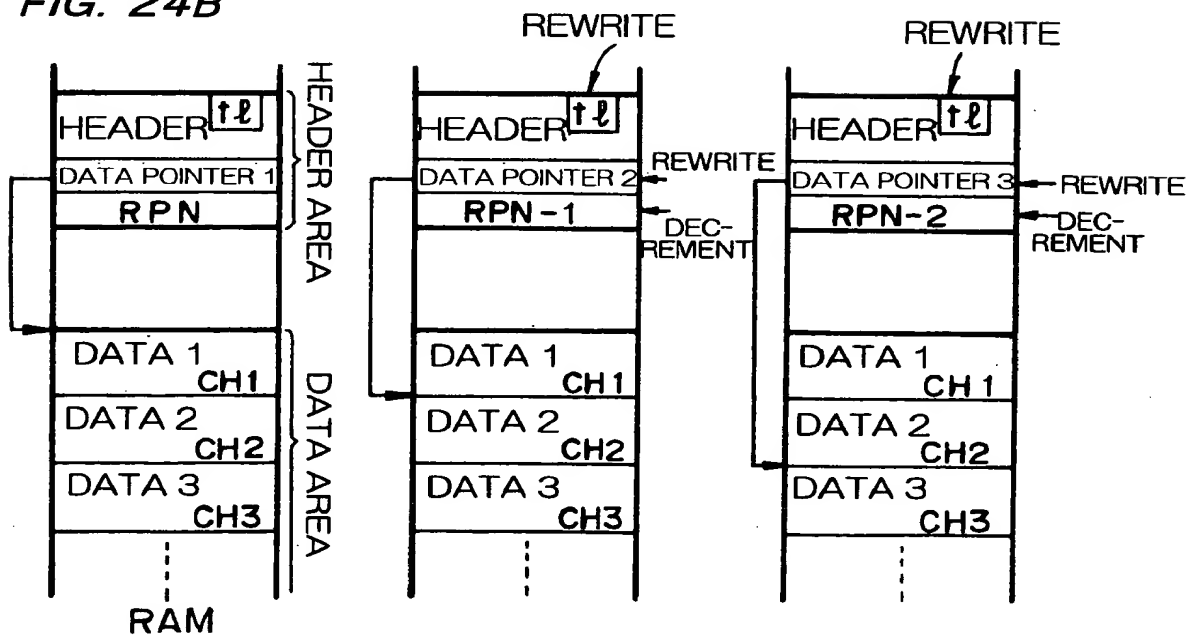


FIG. 25A

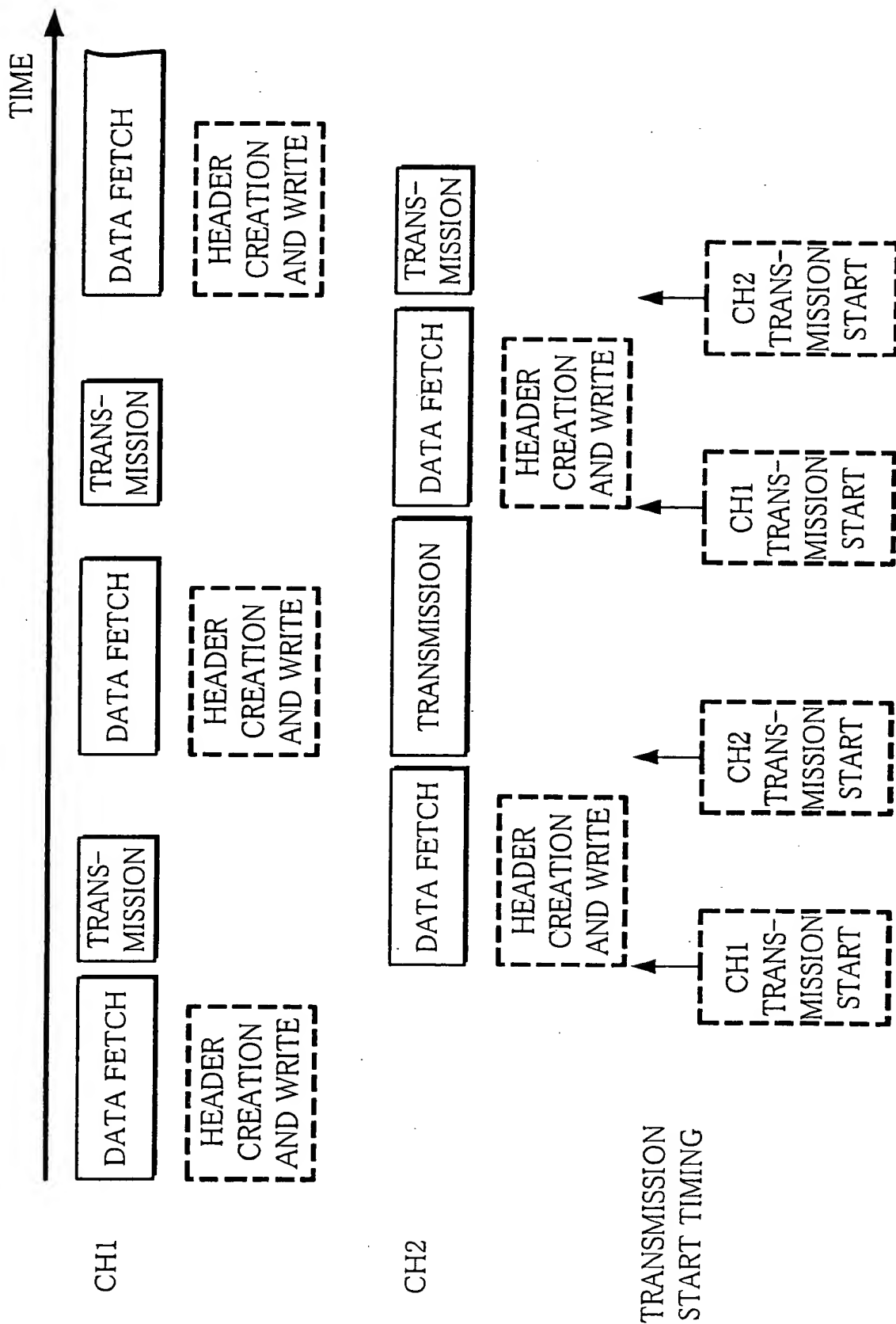


FIG.25B

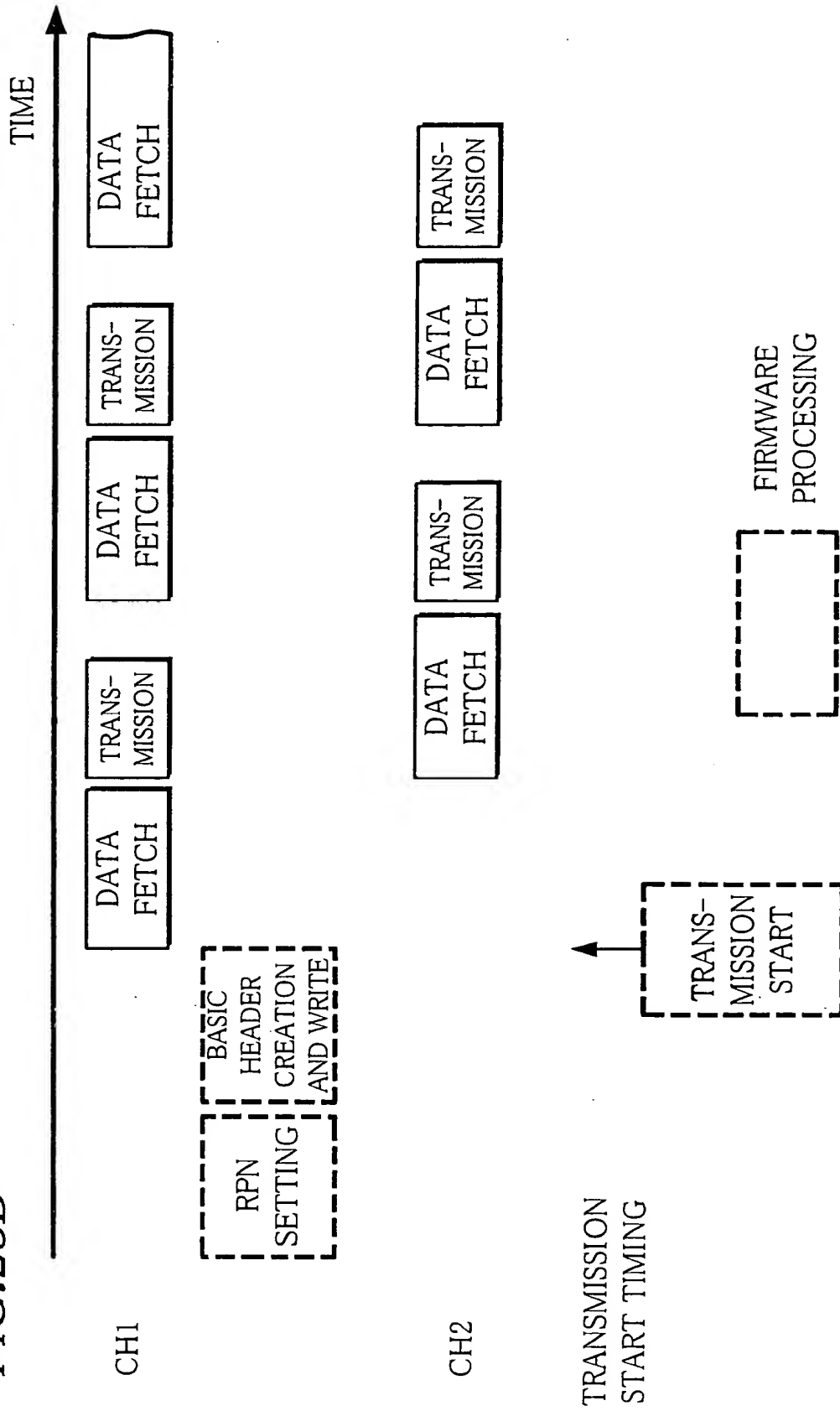
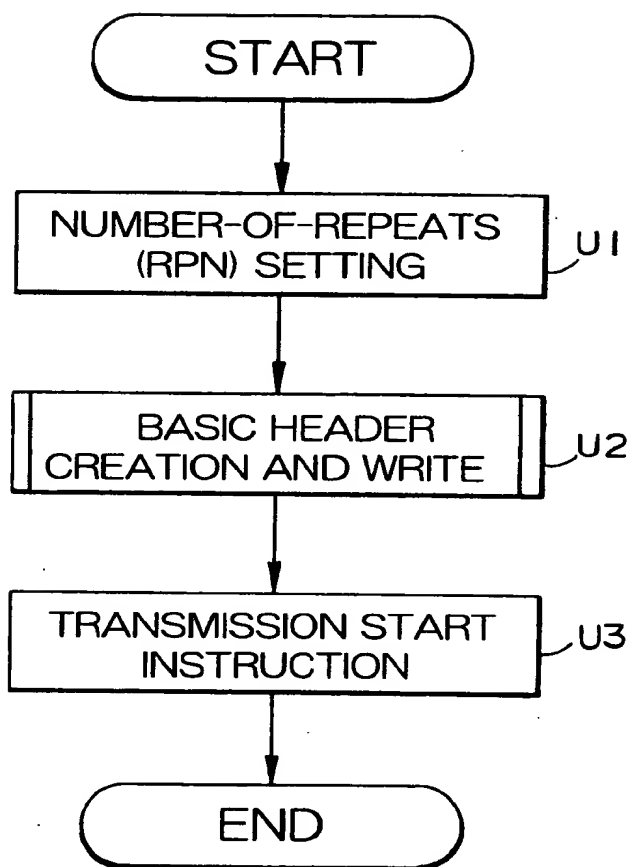
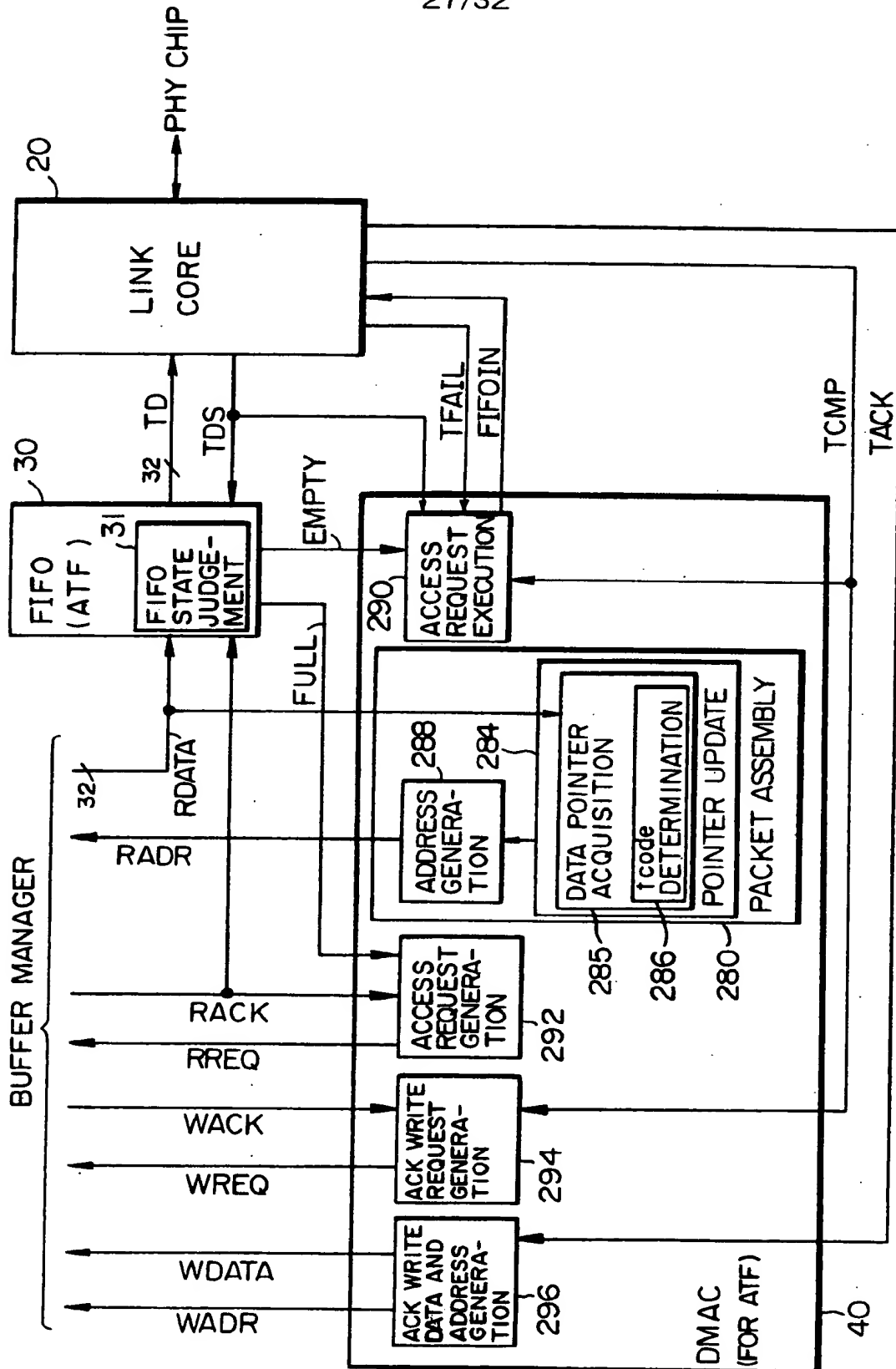


FIG. 26



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FIG. 27



The timing diagram illustrates the sequence of events for a read cycle in the 6800 microprocessor. The signals shown are:

- TSTART**: The start of the first clock cycle.
- FIFOIN**: The input to the FIFO buffer, which is active during the first clock cycle.
- TD**: The data bus, which carries the header information (H0, H1, H2, H3) and the data (D0, D1, D2).
- TDS**: The data strobe, which is active during the first clock cycle.
- TCMP**: The compare signal, which is active during the first clock cycle.
- TACK**: The acknowledge signal, which is active during the first clock cycle.
- EMPTY**: The empty signal, which is active during the first clock cycle.
- FIFO COUNT FULL**: The FIFO count full signal, which is active during the first clock cycle.
- RREQ**: The read request signal, which is active during the first clock cycle.
- RACK**: The read acknowledge signal, which is active during the first clock cycle.
- RADR**: The read address, which is active during the first clock cycle.
- RDATA**: The read data, which is active during the first clock cycle.
- WREQ**: The write request signal, which is active during the first clock cycle.
- WACK**: The write acknowledge signal, which is active during the first clock cycle.
- WADR**: The write address, which is active during the first clock cycle.
- WDATA**: The write data, which is active during the first clock cycle.

The diagram shows the timing of these signals relative to the clock cycles. The first clock cycle is the most critical, as it contains the header information and the data strobe. The subsequent clock cycles show the data transfer and the acknowledgment signals.

FIG. 29A

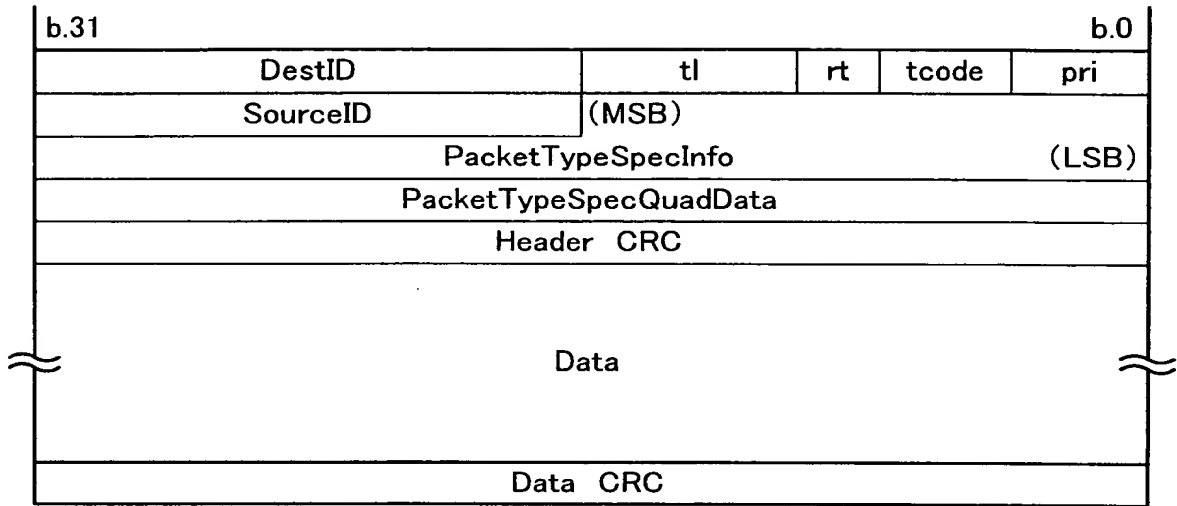


FIG. 29B

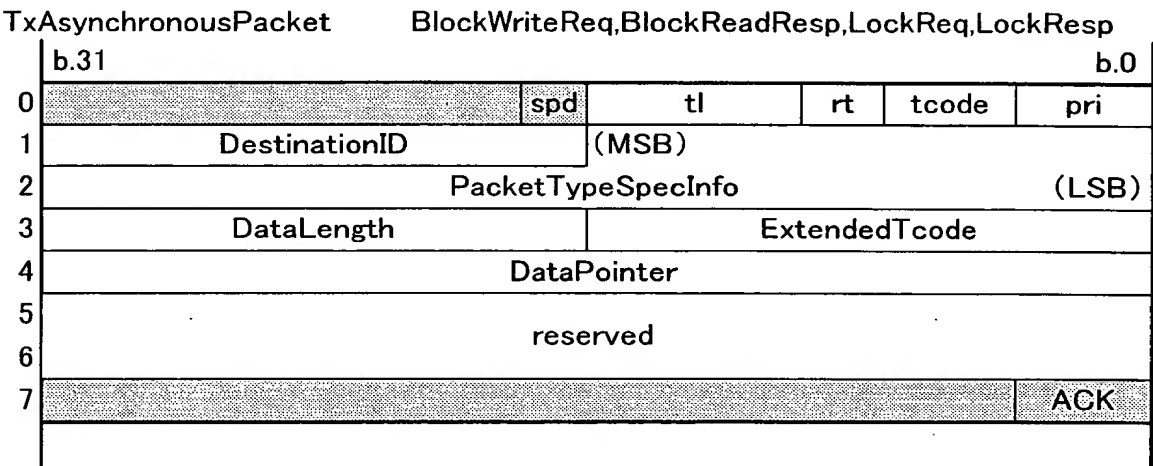


FIG. 30A

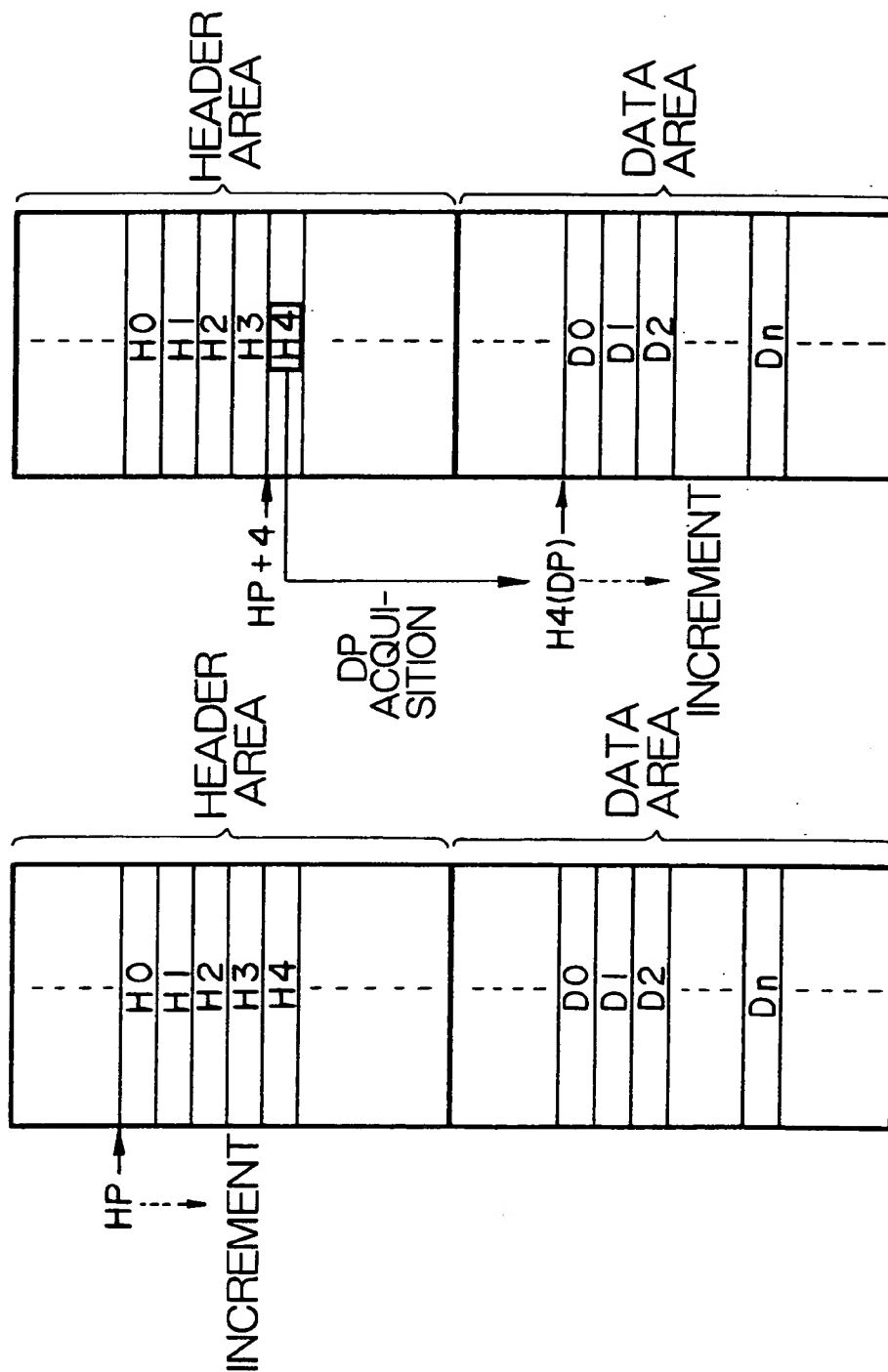
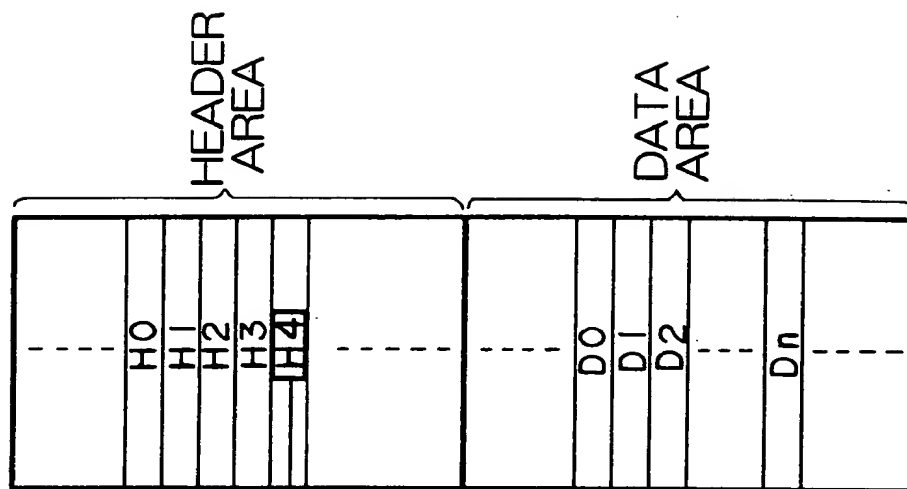


FIG. 30B



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FIG. 31A

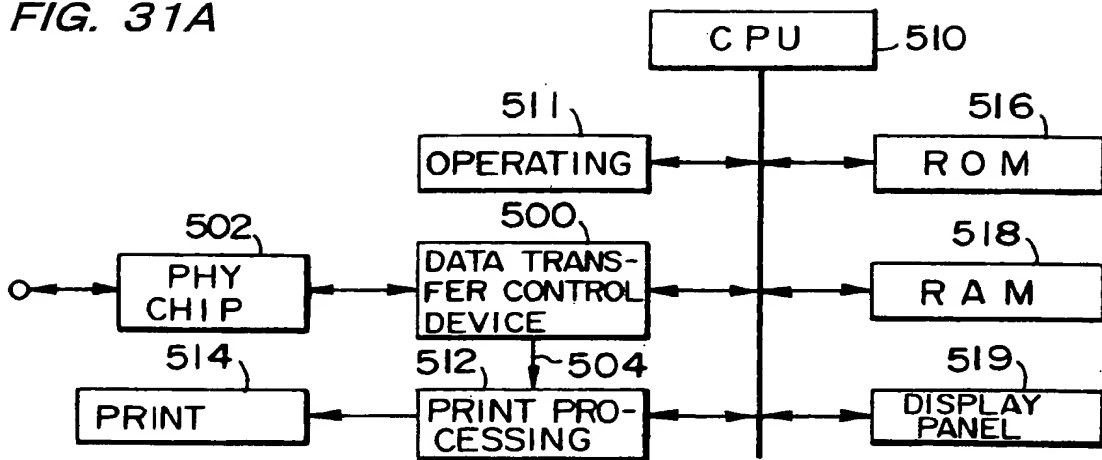


FIG. 31B

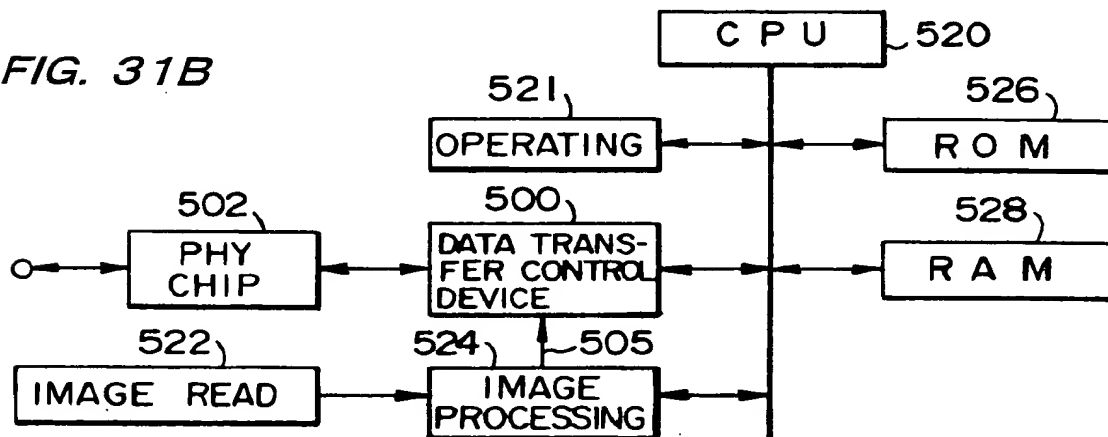


FIG. 31C

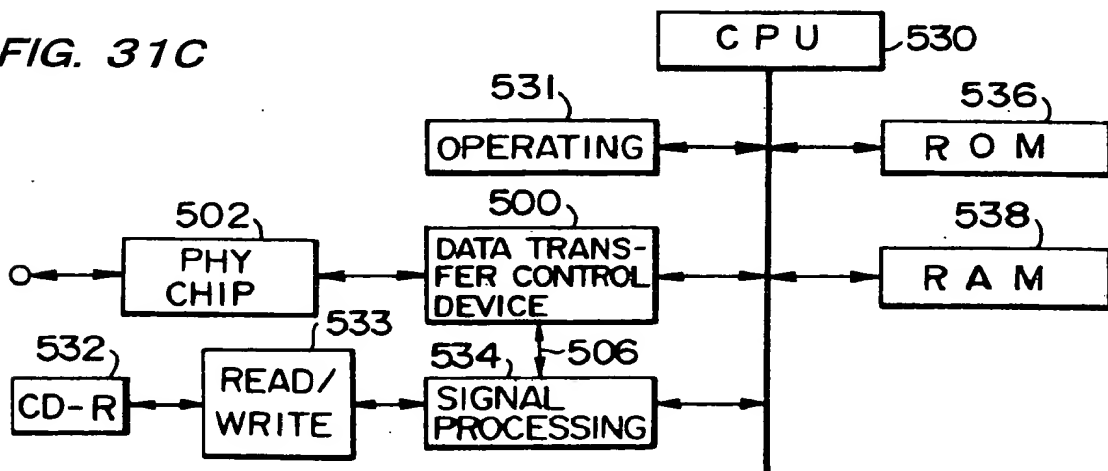


FIG. 32A

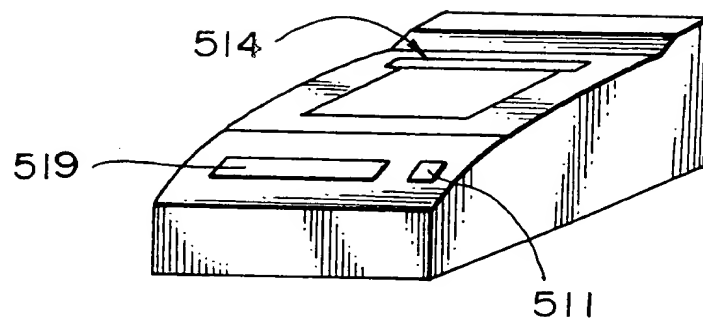


FIG. 32B

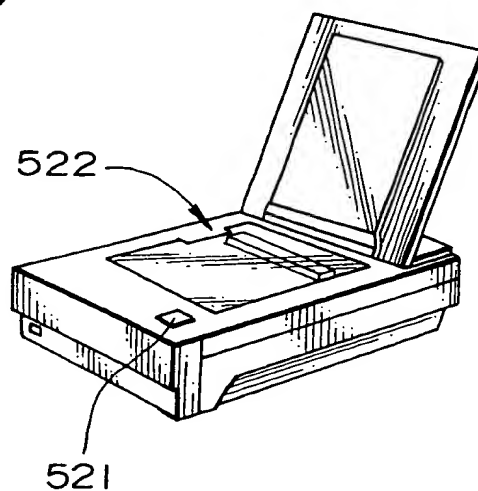


FIG. 32C

